**Problem 1.** This problem concerns an 8 × 8 array multiplier.

1. Draw the organization of an 8 × 8 array multiplier and calculate how many full adders, half adders, and AND gates are required.
2. Draw state chart (ASM)of the operation.

**Problem 2.** This problem involves the design of a BCD-to-binary converter. Initially a 3-digit BCD number is placed in the *A* register. When a start signal is received, conversion to binary takes place and the the resulting register is placed in the *B* register. At each step of the conversion the entire BCD number (along with the binary number) is shifted one place to the right. If the result in a given decade is greater than or equal to 1000, the correct circuit subtracts 0011 from that decade. (If the result is less than 1000, the correction circuit leaves the contents of the decade unchanged.) A shift counter is provided to count the number of shifts. When conversion is complete the maximum value of *B* (10-bits) will be 999 (in binary).

1. Illustrate the algorithm starting with the BCD number 857, showing *A* and *B* at each step.
2. Draw the block diagram of the BCD-to-binary converter.

Draw a state diagram of the control circuit (3 states). Use the following control signals: *St*: start conversion; *Sh*: shift right; *Co*: subtract correction if necessary; and *C9*: counter is in state 9, or *C10*: counter is in state 10. (Use either *C9* or *C10* but not both.) (d) Write a Verilog description of the system